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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,527	08/31/2000	Vladimir Berezin	08305/078001/99-23	4646

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,527	BEREZIN ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,11-16 and 22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,11-16 and 22-28* is/are rejected.

7)☒ Claim(s) *1-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 10, 2005, has been entered.

Response to Arguments

2. The amendment to claim 1 has overcome the rejection. Claims 1-3, 5, 6, 8, and 9 are allowed.

3. The indicated allowability of claims 7, 11-13, and 22-28 is withdrawn in view of the Kuroda reference. Rejections based on the reference follow.

Claim Objections

4. Claims 1-3, 5, 6, 8, and 9 are objected to because "said first bias line provides power a said second transistor" on line 12 of claim 1 is unclear. For examination purposes, the claim will

be treated as if it reads, "said first bias line provides power to a said second transistor".

Appropriate correction is required.

5. The amendment to claim 27 has overcome the objection presented in the previous Office action. The objection is withdrawn.

Claim Rejections - 35 USC § 112

6. The amendment to claim 28 has overcome the rejection under 35 U.S.C. 112, first paragraph. The rejection is withdrawn.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hack (U.S. Patent No. 5,153,420).

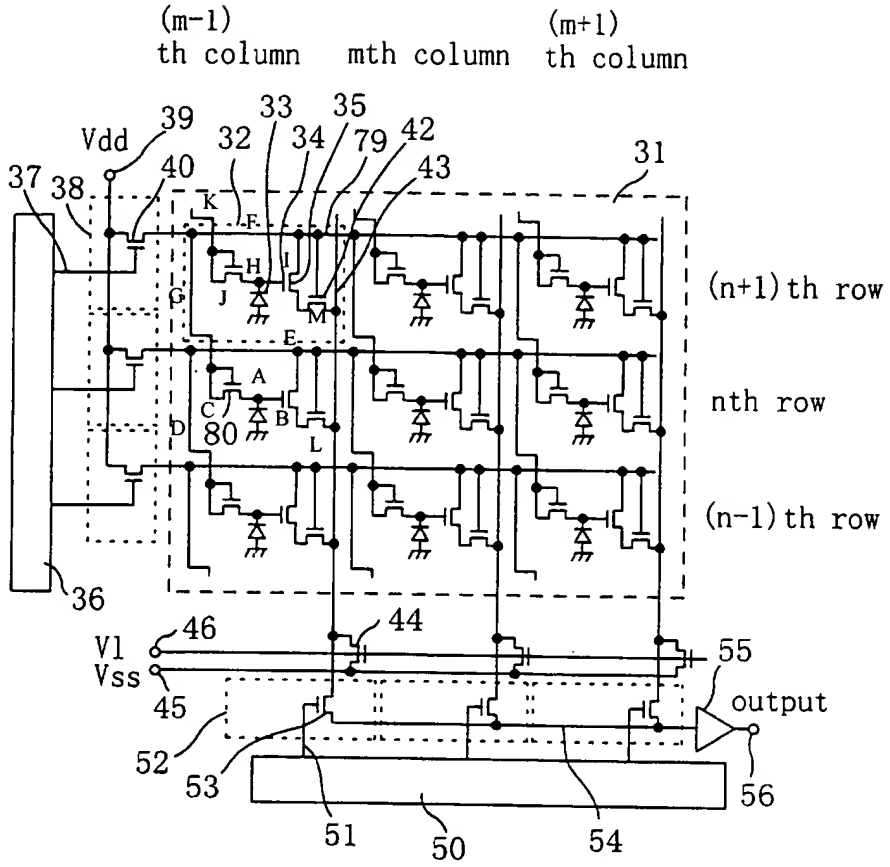
Regarding **claim 14**, Hack discloses, as shown in figures 1 and 2:

> an array of pixels, each pixel (cell 10) comprising a photoreceptor (photosensor circuit region 12; see column 4, lines 27), and at least first (18) and second (30) transistors associated with said photoreceptor in said each pixel, each first transistor of each pixel providing a same pixel function and each second transistor of each pixel providing a same pixel function, said first transistor of a first pixel connected to receive power from a first power supply source (the row-specific output of addressing means 6) over a first line (A_n), and said second transistor of said first pixel connected to receive power from a second power supply source (the row-specific output of addressing means 6) over a second line (A_{n+1}) separate from said first power supply line (the lines are independently controlled by addressing means; see column 5, lines 26-33), wherein said first transistor of said first pixel and said second transistor of a second pixel are connected to said first line (Figure 1 shows that the pixels repeat; see column 5, lines 62-63, and column 6, lines 6-7).

Regarding **claim 15**, Hack discloses:

> said first transistor and said second transistor of each pixel have drains which are not electrically connected (see Figure 2).

9. The following figure includes the labels that will be used in the Kuroda rejections under 35 U.S.C. 102 and 103:



10. Claims 22-~~28~~ are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroda (U.S. Patent No. 6,512,543).

Regarding **claim 22**, Kuroda discloses an image sensor, comprising:

a first pixel (D), said first pixel comprising a first photoreceptor (A), a first follower transistor (B; see column 6, lines 57-58) having a gate connected to said first photoreceptor, a drain of said first follower transistor connected to a first line (E), and a first reset transistor (C; see column 9, lines 19-20), a drain of said first reset transistor connected to a second line (F); and

a second pixel (G), said second pixel comprising a second photoreceptor (H), a second follower transistor (I) having a gate connected to said second photoreceptor, a drain of said second follower transistor connected to said second line (F), and a second reset transistor (J), a drain of said second reset transistor connected to a third line (K).

Regarding **claim 23**, Kuroda discloses:

said first, second, and third lines are power supply lines (power is supplied from Vdd via row-driving transistors 40).

Regarding **claim 24**, Kuroda discloses:

said first, second, and third lines are connected to a same power supply (power is supplied from Vdd via row-driving transistors 40).

Regarding **claim 25**, Kuroda discloses:

said first pixel further comprises a first select transistor (L) connected to said first follower transistor, said second pixel further comprises a second select transistor (M) connected to said second follower transistor.

Regarding **claim 26**, Kuroda discloses:

said second select transistor and said first reset transistor each have a gate connected to a first reset/select line (F).

Regarding **claim 27**, Kuroda discloses:

a gate of said first selected transistor is connected to a second reset/select line (E).

Regarding **claim 28**, Kuroda discloses:

a gate of said second reset transistor is connected to a third reset/select line (K).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 7, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda.

Regarding **claim 7**, Kuroda discloses:

a plurality of pixels (D, G, etc.) formed of transistors (B, C, I, J, L, M, etc.), each pixel associated with accepting a pixel of an image, and each pixel comprising:

a photoreceptor (A and H) therein,

an in-pixel follower transistor (B and I) connected to said photoreceptor,

an in pixel select transistor (L and M; see column 9, lines 50-51) connected to said follower transistor,

and an in pixel reset transistor (C and J; see column 6, lines 57-58) which controls applying a reset level;

a first bias line (E) providing power to at least one of said transistors (B) for a first pixel (D); and

a second bias line (F) providing power to another of said transistors (C) different than said one of said transistors of said first pixel, such that said one and said another transistors are separately powered by separate bias lines;

wherein said second bias line (F) is connected commonly to a first plurality of follower transistors (I) in a first row of said pixels (G) and a second plurality of reset transistors (C) in a second row of pixels (D) different than said first row of pixels.

Kuroda is silent with regard to the pixels being formed with CMOS techniques.

Official Notice is taken that it is well known in the art to form pixels with CMOS techniques. An advantage of doing so is that the resulting image sensor has a lower noise level

than, for example, a CCD image sensor. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kuroda's image sensor formed with CMOS techniques.

Regarding **claim 11**, Kuroda discloses:

> said photoreceptor (A) is connected between a reset transistor (C) and a follower transistor (B).

Regarding **claim 12**, Kuroda discloses:

> a dynamic mode read out transistor (selected row driving transistor 40; column 9, line 41) associated with at least one of said bias lines, and allowing said at least one bias line to be active for only a part of a frame period (see chart 66 in Figure 5 and column 9, lines 36-38).

14. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Miyawaki (U.S. Patent Application Publication No. 2002/0001037).

Claim 13 may be treated like claim 10. However, Kuroda is silent with regard to referencing pixels to a ground reference and then floating the pixels.

Miywaki discloses the image sensor shown in Figure 5, wherein:

> a connection (7) which is configured such that when said connection is activated said pixels (S) are referenced to a ground reference (paragraph 0130) and when said pixels are floated (paragraph 0130).

An advantage of grounding and removing pixels is that accumulated charge on a column output line may be removed, thus reducing noise. For this reason, it would have been obvious to one of ordinary skill in the art to have Kuroda's sensor ground and float a pixel connection line.

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hack in view of Okamoto (U.S. Patent No. 6,580,063).

Claim 16 may be treated like claim 14. However, Hack is silent with regard to including a steady-state current generator that switches between grounded columns and floating columns.

Okamoto discloses an image sensor, including:

> a steady state current generator (current source 809; see column 1, lines 37-38) for providing a first mode connecting columns to ground (column 1, lines 37-43) and a second mode which provides floating columns (activation of bias line 815 occurs at a specific time during the operation, as stated in column 2, lines 11-19; it is therefore inherent that a time exists when the line is inactive and the columns are floating).

An advantage of using such a current source is that the output signals from the pixels may be amplified as each column is read out. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Hack's image sensor include a switchable steady-state current generator, such as the one described by Okamoto.

Allowable Subject Matter

16. Claims 1-3, 5, 6, 8, and 9 are allowed.

Regarding **claims 1-3, 5, 6, 8, and 9**, no prior art could be located that teaches or fairly suggests a plurality of pixels, wherein a first bias line provides power to at least a first transistor in a first pixel and a second transistor in a second pixel, a second bias line provides power to a second transistor of the first pixel and a first transistor of a third pixel, wherein a gate of the reset transistor of the first pixel a gate of the select transistor of a different pixel are connected to a first reset/select line.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The examiner can normally be reached Monday through Friday from 9:00 A.M. to 5:30 P.M. eastern daylight time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu, can be reached at (571) 272-7320. The fax phone number for the organization where this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JTW
JTW
November 15, 2005

NGOC-YEN VU
PRIMARY EXAMINER